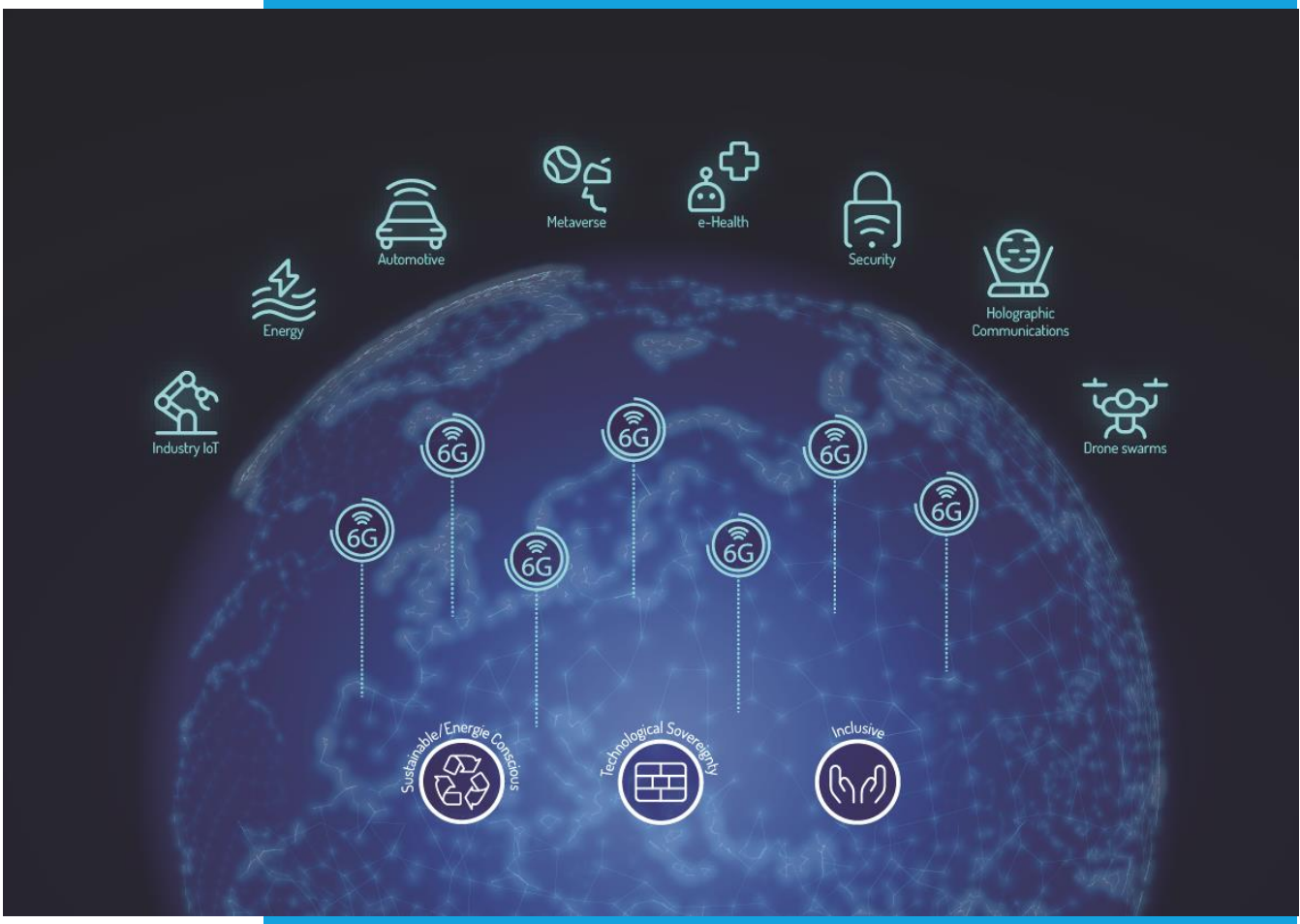
6G Smart Networks and Services Industry Association (6G-IA)



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Position paper

RESEARCH PRIORITIES ON MICROELECTRONICS FOR 6G NETWORKS R&I ACTIVITIES

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6G SNS IA

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1. INTRODUCTION

Similarly to other regions (e.g., USA), the EU has recognised microelectronics as a strategic industrial domain, both from an economic and political perspective. In the wake of the US "Chips and Science Act"[1] aiming at securing US industrial lead and critical supply chains, the EU adopted in July 2023 the "Chips Act"[2], aiming at reinforcing EU excellence and industrial capabilities by injecting at least € 43 billions of private and public investments targeting to secure the supply chains.

Whilst these initiatives cover microelectronic application beyond the sole telecommunication sector, this domain is expected to significantly contribute to their respective objectives. As an example, the US has earmarked $ 1,5 billion only for chipsets relevant for wireless communication systems. In Europe, the telecom and microelectronic sectors have been working in cooperation for already several years and have produced the COREnect roadmap[3], identifying the strategic issues at stake for Europe, which will be further exacerbated by the move of communication infrastructures towards 6G, as expected by the end of the decade. In that context, Commissioner Breton recalled the importance of telecom as a lead market for semiconductors at the launch event of the Chips Joint Undertaking[4]: "We will involve not only the traditional semiconductor industry but also key verticals such as automotive, industrial, and telecommunications."

Against this background, this the present position paper provides a picture of the current 6G vision and developments in Europe and how they may influence or require specific microelectronics developments and priorities for funding of future R&I actions. It is elaborated based on presentations that took place at a dedicated workshop with a number of experts, that took place on 16 October 2023, with the objective of stimulating possible joint/strategic cooperation, notably through structured collaboration between the Chips (Chips JU) Act (CA) and the Smart Network and Services (SNS JU) Joint Undertakings. This workshop was hence supported by key players from both the microelectronics and the communication/networking R&I ecosystems in Europe as well as representatives from the EC.

[1] https://www.whitehouse.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china/

[2] https://ec.europa.eu/commission/presscorner/detail/en/ip_23_4518

[3] https://www.corenect.eu/roadmap

[4] https://ec.europa.eu/commission/presscorner/detail/en/SPEECH_23_6216

2. 6G APPLICATION ASPECTS

In Europe, the 6G vision and use cases are largely driven by the Hexa-X and Hexa-X-II flagship projects as well as related SNS Stream B projects. These results are well reflected in the ongoing standardization work from ITU-R within the Framework Recommendation for IMT 2030 that was completed in June 2023 and finally adopted last November last[5]. The figure below extracted from this recommendation ITU document reflects how the 5G use cases are extended, what new use cases are considered and what horizontal non-functional properties are framing the development of 6G.

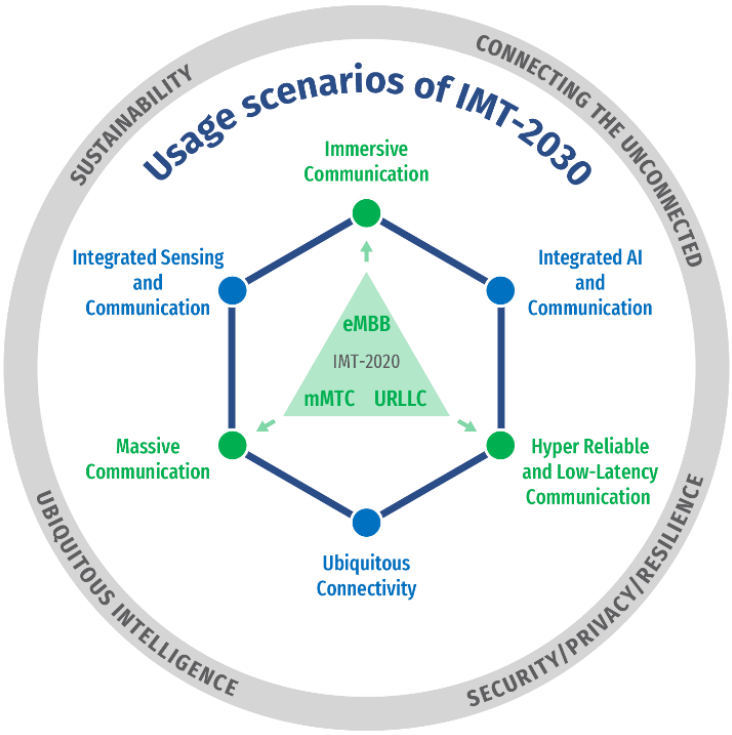

Figure 1: Proposed ITU Framework Scenario for IMT 2030 capabilities

Whilst 5G application domain has already largely contributed to the development of new classes and capabilities of chipsets in the mobile communications domains (e.g. for integrated RFIC's capable of handling mm Wave communications at low cost), 6G will push the envelope much further to enable new classes of applications, requiring in turn specific developments for underpinning enabling technologies. The workshop confirmed the need for European industry to ensure lead in sustainable and trusted 6G network technologies that will emerge towards the end of the decade and underpinned by the new set of innovative applications and architectures discussed below. This is considered particularly critical for Europe to keep a lead position in 6G considering the heavily subsidized

[5] ITU-R M.2160, November 2023, https://www.itu.int/en/ITU-R/study-groups/rsg5/rwp5d/imt-2030/Pages/default.aspx

competition emerging from Asian, Indian and US actors. In that context, mastering critical secure Digital and RF chips design and production is seen as a key condition for competitiveness and technological sovereignty.

Main new discussed use cases at the workshop include:

- The use of higher frequency spectrum above 71GHz which is not available in current 5G standards. Sub-THz communications, above 90GHz, is contemplated for a range of applications such as "fibre like" backhaul (to support network densification) or multipoint access in industrial or high-density scenarios. Targeted applications for 6G networks will explore new frequency spectra, such V-, E-, W-, D-bands, so from 60 GHz to 170 GHz, with the most immediate challenge being to unleash the D Band potential (E band existing solutions for backhaul). Eventually, the 300 GHz will also be of interest for Tbps connectivity target. This in turn requires the development of new technological capabilities covering very wide bandwidth with minimal losses, alleviating frequency dependent impairments, and making available high-power amplifiers with optimised non linearities as typical issues. The range of spectrum to be covered also requires efficient integration of heterogeneous technologies. Such technologies are not mature today and heavily researched in the various 6G initiatives in the world. Several microelectronics technologies may be contemplated for this class of use cases (FDSOI, GaN, InP, SiGe… with different performance characteristics as a function of the operating frequency) whilst R&I in this domain is still low TRL. Such high frequencies have demonstrated to be compatible with silicon and semiconductor technologies mastered in Europe and a challenge will be to bring them beyond the PoC stage and be efficiently deployed through multi technology modules with RF, digital and FEM (Front End Modules) integration.
- The addition of upper mid-band spectrum "FR3" (7-24GHz) which may be aggregated to support higher data rate for 6G mobile devices whilst making possible intelligent sharing with incumbent services will require continued progress into the "Angstrom" era of CMOS to keep up with demands for low power compute/high data rates/capacity and (AI assisted) signal processing to maximise sharing capabilities. This spectral range is already well used by communication applications, notably for satellite communications (heavy use of the 10 – 15 GHz in Europe with primary status). As such, it is expected that higher TRL can be contemplated for the underlying enabling techs. Optimisation of spectrum usage would also benefit from full duplex operations (access points to devices) which requires technologies for self-interference cancellation. PA consumption is an important factor, as it must produce from 10 mW to 2W output power, depending on the use-case, potentially more for infrastructure. With efficiency in the 50% range in sub 6Ghz, improvement capabilities (both from architecture and use of efficient tech like GaN) are significant, also in view of realizing better energy efficiency targets. This domain may be considered for reinforcing European positions for mm Wave mid to high bands, as European foundries may be well adapted to such markets.
- New application like Joint Communication and Sensing (JCAS) requires integration of heterogeneous technologies, very wideband transceivers (>5GHz at Baseband), and support of moderate to high spectral efficiencies. R&I may lead towards combined use

of the same waveform (e.g. OFDM for the two applications) which imposes different requirements on the underlying transceivers and hence extra complexity. The trusted knowledge of localization of users, devices, or any type of equipment is a generic question for an advanced network. High precision ranging and positioning can be made available by specific technical means like GNSS or UWB but can also be derived from specific properties of RF communication, that can be enhanced with specific analog and digital processes at low power level including passive radars. On top of this the ongoing convergence of communication and sensing is expected to become a 6G feature, where JCAS is considered a key new enabler – implying also **converged front-ends, transceivers and digital signal processing,** whilst security and trust considerations may require strict separation of both the sensing and communication concerns such that access to the sensing part can be adequately restricted. This will also drive requirements on the hardware and integration both at the device, circuit and packaging level.

- Sophisticated industrial applications will drive the demand for integrated sensors and RF, optical and MEMS devices. Key requirements in this domain include larger data processing capabilities to cope with the bulk of edge data, integrated AI/ML processing for fast low latency filtering, and battery-less device capabilities for zero energy IoT devices. A particular challenge is that the power supply of the associated communicating modules can be operated at close to zero energy cost. Efforts must be put on the power consumption of the RF system in use, notably in the architecture of the RF transceiver to use innovative mechanisms to limit the energy. 1pJ/bit is commonly taken as a target. Novel substrates with very low leakage may be considered and reinforce the ultra-low-power expertise of Europe (e.g. Bluetooth and UWB).
- Higher data rates and lower latency use case requirements further drive needs for SoCs that are designed to handle them. They integrate various functions such as digital signal processing, memory, and power management into a single chip, making them more efficient and cost-effective. SoC contemplated by European industry today are primarily targeting Layer 1 communication capabilities of radio access networks (RAN), whilst there is no intention at this stage to develop higher layer capabilities towards full modem implementation, as it is available from the US (Qualcomm) and Asia (Samsung, HiSilicon). Though not addressed at the workshop, a European approach towards developing mass market 6G user equipment's may be worth considering as this drives demand for 2nm chipsets volumes, generates demand towards foundries and supports EU sovereignty.

The workshop and subsequent stakeholders' contributions concentrated primarily on Layer 1 aspects and physical implementation, including related development tools. In that respect, very low energy consumption appeared as a critical cross domain requirement with trust and security being another important cross domain aspect. Computing was also addressed as an important aspect, though with less emphasis than L1 issues.

3. 6G ARCHITECTURAL ASPECTS

6G current developments are considering several architectural implementations that are expected to significantly improve network performance characteristics whilst requiring specific progress of the microelectronics supporting technology. The workshop addressed notably:

6G as a communication fabric requires the integration of a multiplicity of access networks, cellular or not, ranging from satellites (and Non-Terrestrial Networks - NTN) to optical terminations. This requires enabling technologies that can handle the integration of low-cost discrete technology for transmit arrays and the capabilities to integrate heterogeneous multiple frequency bands. Waveform flexibility emerges as a topic enabling ad-hoc implementation of channel/traffic optimized waveforms potentially also driving unification between TN and NTN accesses. Technology is required to realize high digital integration and low power consumption as well as high power as needed for small antenna arrays.

Cell-based (CB) and cell-free (CF) networks

Cell-free based networks with UE's connected to a multiplicity of access points (AP's) connected in turn to one or several processing units emerges a concept potentially providing very robust transmission with combination of signals originating from several AP's. The concept however requires solving the multiple AP operations with limited fronthaul capacity, the energy dissipation with simple processing and tight synchronization. As estimation of position and orientation in cell-free architectures emerges as a critical requirement, equal privacy concerns to JCAS arise here, and trustworthiness emerges as an issue to address as well. In addition, such architectures will require a high level of synchronization between APs, as well as parameters sharing for better individual configuration, and more studies on Power Amplifier (PA) linearity thanks to AI-aided processing.

MU MIMO, M-MIMO

MIMO systems with multi beam capability through patch array implementation require sophisticated transceiver and digital processing, to realize accurate beam steering and multiple beam generation. Technologies for beamforming are critical in that respect, e.g. CMOS or optical. Antenna arrays are key for future networks topologies to provide more directive connection link between UE and AP's. Beam will be implemented with MIMO deployment, able to address several users in the same cell. Making them dynamically reconfigurable, multi-user, and able to operate in mobility context is mandatory to address 6G goals. The design of phase-shift array chips needs be supported with semiconductor technology achieving the 3-fold goal of low cost (even with hundreds of antenna patches), high-performance (output power for the Tx and low NF for the Rx), and low-power consumption/high energy efficiency as possible. This will, especially for the higher bands, require heterogeneous integration and advanced packaging. It may be expected that high-precision beamforming making use of compact antenna array technologies will lead the way to mix modalities, like addressing sub-6GHz bands as well as mm Wave ones.

AI/ML

Flexible 6G use cases and operations is supported by AI/ML as a technology to be integrated at various levels of the 6G platform. 6G is currently being contemplated as an "AI native platform" (i.e. with systematic capabilities to exploit the high data volumes generated from within or outside the platform). This may have multiple impacts at different levels, such as:

i) the need to have powerful GPU technology capable of AI/ML assisted intelligent/reconfigurable management of radio waveforms as a function of traffic/channel characteristics, also enabling unification with NTN access capabilities (see above),

ii) processing capabilities as required to support AI/ML assisted security from an end to end or local perspective,

iii) processing capabilities for real-time AI/ML assisted function placement/execution as a function of the use case scenarios, etc. In the long term, AI/ML processing based on GPU may reach limits whilst other technologies like analog neural network processing bear promises of performance improvement by a factor of 200 with low energy consumption compared to existing technologies. These techniques may be studied in the context of Radio Interfaces for maturity within the 6G compatible time frame (2028-30).

Reflective Intelligent Surfaces (RIS)

The advent of new level of efficiency in interference/spectrum control for deployment scenarios based on RIS (Reflective Intelligent Surfaces) requires the availability of intelligent (AI/ML driven) surfaces build using metamaterials also with the objective of reducing EMF exposure of people.

RIS are benefiting from reconfiguration features that are possible on large antenna arrays, acting as a reflecting or transmitting surface that can dynamically modify the beam direction depending on the BS/AP and UE relative position. Stand-alone deployment acting as a passive-like component in the network, requires embedded low-power intelligence featuring sensing and positioning ability, notably at very low power consumption. New algorithms supported by energy efficient hardware are needed.

Virtualisation and disaggregation

The move towards virtualised and disaggregated networks, already started with 5G, is expected to continue and be amplified by the emergence of 6G. This is a domain that is currently stimulating many initiatives originating from non-EU microelectronics/software/cloud actors with a clear intention to compete with established EU networking technological leadership. In view of sovereignty objectives, it is of interest to stimulate and enhance EU capabilities in this domain, whilst avoiding lock in at the level of the virtualisation underlying microelectronics/software platforms currently dominated by a handful of non-EU players. Europe should hence strive to expand its own capabilities in the digital processing domain. Microelectronics requirements in that respect are multiple and characterised by:

i) the need for software implementations to reach performance levels on par with classical hardware-based implementations, especially for real time radio functions where generic purpose processors may not be enough. The need to avail from accelerators for multiple critical functions that may be incorporated in various platforms with virtualised implementations is important in that context,

ii) the need to avail from open multi source supply chains, RISC-V technology developments may be contemplated in that respect,

iii) the need to optimise energy efficiency at data processing level (in addition to what may be achieved through intelligent management of resources, e.g. RIC in Open RAN), whilst software implementation may lead to higher energy consumption.

Disaggregation is also driving specific requirements at edge and extreme edge, as native AI will support user experience and service delivery, while taking into consideration that the resources at UE have to remain limited for cost and power consumption reasons. Data centre SoC technology cannot be reused and require considering specific AI accelerators and fabrics that can act as local compute nodes (e.g. low-energy analogue neural network processing) or even integrate with the sensors in the devices to enable optimal use of scarce communication resources and power. Use of analogue neural networks processing needs to be studied.

NB: The above topics on radio system architectures are subject of several SNS projects that are also dealing with microelectronic components.

4. TOWARDS EUROPEAN CAPABILITIES FOR 6G ENABLING TECHNOLOGIES

From a general viewpoint, 5G towards 6G Digital Front End (DFE), compute, baseband, AI and DSP chips, chiplets and chipsets (System on Chip, SoC) are quasi leading-edge technology at 3nm node size and will be 2nm technology based by 6G era. 6G chips also need to enable 20x current network performance whilst reducing by 50% mobile systems energy consumption. This calls for active product-oriented R&D&I seeking for the needed technologies, architectures and implementations.

Reaching the 6G performance and architectural capabilities exposed above require, especially at the level of new generation of transceivers, to master 3 classes of technologies:

- ***computing*** (CMOS, FDSOI),
- ***RF*** (RF CMOS, RF SOI, FD-SOI, GaN-on-SiC, GaN-on-Si, InP, InP on Si, SiGeBiCMOS, SiGebipolar), and
- ***power generation technologies*** (GaN-on-SiC, GaN-on-Si, BCD, LDMOS).

Europe has strong assets in these 3 domains, which require however to master a complete life cycle in architecture, design, integration, new devices and process technologies and packaging, which drives in turn a strong and early cooperation on microelectronics, telecom, hardware and software developments.

Smartphone processors and computer markets are driving digital processing advances with integration levels in the 7-nm and 5-nm range with 3-nm and 2-nm on the horizon. Europe has no capability in these domains, but opportunities are being created (supply chain issues) e.g. in the IPCEI context potentially leading to EU design and fabless capabilities. It does not address only the digital part of the design but needs to integrate the analogue/mixed signal part (ADC/DAC) which need to be more integrated with the DSP logic to minimize power consumption. Reaching the "COREnect vision" of compute and store, connect and communicate, sense and power requires in addition adequate design platforms capable for hybridization of various processes with optimized technological choices. In that context, single chip implementation is not seen as the way to go, but rather a chiplet approach with high heterogeneity of implemented technologies. From that perspective, it is noted that the 3 key European RTO's have complementary expertise in heterogeneous integration.

From an edge and device perspective (IoT) low power and low cost with capabilities for integrated sensing, capture, monitoring, are key to unleash markets driven by volumes, going beyond pure smartphone device markets. Key European assets in this domain include micro-controllers and sensors, but processing capabilities may need developments. The current efforts developed in the automotive domain based on RISC-V technology for the SDV (Software Defined Vehicle) might potentially form a baseline to capitalize on. Availability of 2 nm silicon node technology would be an asset to promote and boost demand for 2nm foundry in Europe.

a) Layer 1, Transceiver technologies

From mm Waves mid- to high band, there are many approaches that can be addressed. It is crucial to have a complete multi band perspective at system level to optimize design of components. One path of investigation is to design mm Wave chips that can be reused for various bands. This can be done by considering efficient frequency plans to mutualize frequency generation and make it possible to have frequency synthesizers reusable for different mm Wave bands. On the other, rather than developing complex and power consuming chips for each band, make use of a lower band as a step towards a higher ones : for instance, the 26/28 GHz band chips could be used as intermediate frequency for 60 GHz or 81 GHz band. For sustainability purposes, such a vision would help to reduce the number of chip iteration and focus on the production of some standard IC.

Use of ML/AI for Tx/Rx need to be evaluated for superior 6G performance and low cost, plus low energy consumption solutions. Analog neural networks processing is promising technology for this domain.

Europe has good strengths in the field of co-integration of Digital process and Mixed-Signal/RF front-end, including manufacturing resources, in view of achieving leadership. One can in particular note European know how on:

- BiCMOS
- CMOS FD-SOI
- GaN
- InP

A roadmap for combination of these technologies may help to define next generation Front-Ends.

From the perspective of semiconductor capabilities in relation to the target performance architectural building blocks of 6G, one can mention:

SiGe BiCMOS:

SiGe technology platforms enable high-performance RF Front-End with CMOS integration capabilities. Operating frequencies to above 100 GHz, large bandwidth, low noise, high linearity potential and decent output power in the mm Wave mid- to high band are possible. For node scale, 130-nm are adequate mainly below 60 GHz, and 55-nm may provide much higher frequency performance and of course digital integration. NB: IHP offers foundry services for BiCMOS 250nm and even recently 130nm.

FD-SOI:

Fully Depleted Silicon on Insulator (FDSOI) CMOS can be attractive for both digital (28nm/22nm today, 10nm tomorrow) and analog/RF/mm Wave integration. FT and Fmax are about 300 GHz demonstrated in 28-nm node, FD-SOI may also be considered for on-chip antenna. Moving towards 10 nm is considered.

GaN:

GaN benefits it combines power and high energy efficiency, especially for mmWave. Applications include infrastructure (BS), and cells (SC/PC and AP). Current developments tend to demonstrate its ability to address even higher frequency bands devices showing Fmax of 400GHz, that may be of interest for the D-band/140GHz. Various flavors of GaN implementation exist and power density results in small devices with low parasitic, limiting the losses between drivers and PA, and enabling high quality interstage matching networks.

InP:

InP allows increasing the frequency in use, much above 100 GHz. The gains are higher than with any other technologies Fmax higher than 1 THz have been demoed. Promising use for InP would be D-band/140 GHz, associated to either CMOS or BiCMOS transceivers. Power consumption and number of antenna array element, for a given radiated power is related and InP technology for the PA outperforms any other. Issues may relate to scale and cost.

Integrating these technologies to enable the full capability, including advanced CMOS (10 nm and below) for digital process and modem/baseband with high flexibility is required. European benefits will emerge from hybrid solutions adapted to the required performance power consumption targets.

CMOS is a leading technology for sub-6GHz and mid-band mm Wave applications. When it comes to mid- to high- mm Wave bands, and of course sub-THz ones, the target is to reach tens to hundreds of Gbps connectivity links. Here, there still exists a critical gap to be filled in between system-level architecture ambitions, that have demonstrated high integration way forward, and current technologies that will support these implementations by horizon 2030. Referring to abovementioned 6G goals, efficient high-frequency and expected sustainability targets must be found. Combining transceivers design and its associated antenna arrays will be achieved at the cost of a trade-off on the architecture level and on the technology split: optimizing performance all along the chain by partitioning complexity, specifications and cost, this latter being driven for a major part by the semi-conductor technology.

b) Optical Technologies

Optical capabilities and processing are key in several 6G related aspects:

- In the context of the realization of the network of networks vision, with DSP capabilities needed to terminate optical bearers (e.g. on PON's) and to efficiently interface with transport networks,
- In the context of switching and routing, with optical DSP's, at transport or backhaul level,
- As a scalable and energy efficient technology for beamforming (demoed in several EC projects) and driving further work (potentially under SNS) on Silicon photonics integration,
- As an additional technology to provide the positioning/sensing capabilities of 6G, using Lidar technology as possible complement to Sub THz capabilities.

This in complement to the classical work on optical communications, noting that widest possible penetration of fibre networks including backhaul or IAB for deployment of dense cluster of AP's is beneficial from the capacity, security and sustainability viewpoints.

c) Computing Technologies

As identified by the COREnect project, this is a domain where Europe is not in good position (see also CMOS nodes capabilities above). Computing technologies are particularly important for network virtualization and disaggregation, a trend started with 5G and expected to gain accrued importance with 6G. Main challenges appear today to cover security, energy efficiency and performance especially for Real Time L1 functions such as LDPC coding, packet scheduling… European industry actors, notably SME's, are working on accelerators based on x86 or ARM platforms in complement to larger actors that are developing their own solutions. Availability of such acceleration technology is critical, but

current efforts are also intending to provide interoperability and portability of accelerators across platforms.

In the longer term, analogue neural network processing may support acceleration of up to 200 times the State of the Art and emerges as a good R&I candidate.

Whilst an accelerator centric initiative is of interest as a response to the computing challenges, it may be explored the opportunity/risk/interest of developing additional computing platform for communication systems, e.g. piggybacking on RISC-V developments taking place in other domains, notably in the computing domain. Critical success factor is the possibility of using technology that is not developed for one single application domain but that can find applications in multiple domains (coms, automotive, industry, etc.) and extended to parts of a network computing platform, though probably not too harsh real time computing challenges located close to the antenna and that may not be appropriate for virtualized implementations.

On a), b), c) above, it may be noted that significant design and integration work is currently taking place through implementation of Chips JU (former KDT) projects. Considering mm Wave aspects, major efforts are being invested in the context of automotive applications, but communication may also benefit from these developments. Future work may consider more systematically architectural aspects driven by com networks implementation. On RISC-V, Chips JU is also involved in developing multiple open source building blocks, also considering the Software Defined Vehicle work currently undertaken by the automotive industry.

Considering the efforts invested under the Chips Act to develop/reinforce pilot lines in Europe, and in view of maximizing the opportunities for European presence from design to fabrication, it may be worth considering technologies and technological building blocks of the 6G chain that are directly related to these target pilot lines.

Complementary Issues

Packaging is a key field to reach performances that are expected from an IC. Increasing frequency bands or reducing margin for high efficiency **pushes very much the constraints on package.** This field has been for long left behind in Europe and most packaging activities are today done in Asia, whilst it is a strong factor of performance improvements as well as a high added-value topic. 6G pushes the criticality of packaging one step further because of the heterogeneity of technologies and interconnects that need to come together to make the system work in a sustainable manner.

EDA and design tools are also critical, in view of realizing the best design of circuits potentially avoiding prototyping (e.g. digital twins) for reduced development cycles. EDA is proposed to become a project of its own, using AI as part of the design process and accounting for the integration heterogeneity required to move towards powerful SoC's.

5. POSSIBLE WAY FORWARD

In addition to the discussions on 16.10.23 workshop, extra contributions have been provided offline by the stakeholders, against 24 themes (see Annex 1). These contributions have been submitted in view of better framing the priorities as important subsets of the variety of topics identified above, of defining the work focus, the level of maturity of the target technology, and the implementation modalities through identification of the centre of gravity of the activity (mainly SNS JU or Chips JU).

5.1. GENERAL CONSIDERATIONS.

- Not all the 24 identified topics received the same number of contributions. Most popular topics revolve around the availability of integrated (heterogeneous) and packaged technologies enabling the realization of transceivers and modems. It is proposed to focus in priorities on these topics that have stimulated a higher number of contributions.
- It is however proposed to also consider as high priorities other topics that have received less contributions (e.g. JCAS) but which are indirectly addressed through contributions to other topics.
- Not all the contribution for a given topic do address the same issue. There is a need to clearly frame the topic at the level of downstream specification, should the topic be considered in the context of SNS-Chips JU's cooperation.
- When specified, the target TRL levels are somewhat consistent and in the TRL 3 to 6 region, with the exception of topic 13 "Cost-effective III-V Si for power and low-noise amplifier" (InP and others), which is not expected to be beyond 4 at the end of projects considering that the issue is described as being very low TRL today (1-2). There is hence no clear topic separation "per TRL" between the two JU's.
- SNS vs Chips JU. There are not always clear messages emerging on where the topic must be addressed in priority. For issues with a clear microelectronic fabrication relation (e.g. growing the technology on top of a substrate) the preference goes clearly to the Chips JU. Topics with a more "system content" (e.g. transceiver for sub-THz coms) views are divided between the two JU's. One contribution takes an extreme perspective, i.e. topics of interest should be addressed under SNS because of the telecom application context.
- Methodologies of JU cooperation: very few contributions/suggestions were received on this topic. Several schemes may be conceived:
    - Topic fully addressed by one or the other JU, with loose information channel towards stakeholders of other JU (workshops, webinars, etc.)
    - Topics addressed sequentially, e.g. for issues still requiring lots of system work (cell free nets, etc.-) specification and detailed requirements may be set in SNS, before development of enabling architectures/technologies under Chips JU.
    - Conversely, mature technology already developed in Chips JU could be considered for integration for a complete communication (set of) function(s). This

is the model that has been tentatively developed for the SNS WP 2024 lighthouse project on microelectronics. It requires the identification of a TRL roadmap over time.

- Initiative like calls: a set of complementary topics is defined as constituent of an initiatives, budgeted from both SNS and Chips JU, with part of the components addressed in SNS, some in the Chips JU. Calls may be coordinated (i.e. synergy call) or more loosely organized in time, as a function of the possible launch windows of the calls.
- Parallel treatments: this is suggested by one contribution but may be difficult to organize the complementarity and the coordination.

5.2. RECOMMENDATIONS FOR FUTURE COOPERATION

The submitted contributions clearly majors on future transceivers, integrated heterogeneous technologies, the technologies enabling cost/energy efficient operations at mm Wave and up to D band (as a starting point), and the tools to manufacture such technologies. From the perspective of the received contributions, such an area of work would major on European know how, especially for III-V technologies and CMOS integration, with one weak point being the packaging and integration. It is also interesting to note that such work does not start from scratch, as relevant work is being implemented under both the SNS and Chips JU (and in some IPCEI's to an extent). ***The core proposals hence consist of a joint SNS-Chips coordination, with focus on a consistent subset of complementary topics, extracted from the list of 24 topics listed in Annex 1.*** The table below suggests what such an initiative could include together with the potential timing and priority, with 1 meaning priority for WP 2025 and 2 meaning priority for WP 2026:

Table 1: Possible components of a FEM initiative

Topic[6]	**Focus/justification**	**Anchor JU**	**Priority**
Topic 1. Ultra-high transmit power/system gain beyond 100 GHz	High number of contributions. Core technologies to develop high power/ high gain/low noise transceivers together with their coupling with CMOS digital technology. This is a core building block for power/energy	Chips JU, specs drive from SNS	1, piggybacking on existing work

[6] See Annex 1 for definition of the topic numbers.

	efficient operation at beyond mm Wave frequency bands.		
Topic 2. mmWave Radio integration system in a package, heterogeneous integration	High number of contributions. Focus is on heterogeneity of technologies, their integration and packaging. Not a strong EU point but seen important from the competitiveness perspective.	Chips JU, packaging initiatives	2, deriving from architectural approaches
Topic 3. High throughput capacity/fronthaul 100 Gbps digital data path	Lower number of contributions, but this moves the integration work one step closer of SoC's, which are critical from a competitiveness perspective as these are the devices where the added value is theoretically at its maximum. Moves into the domain of digital function designs, though constrained at layer 1.	SNS JU, system perspective with definition of functions in SoC.	1, need early start from a system perspective, to be continued under 2.
Topic 6. Joint Communication and Sensing	Limited number of contributions but this represents a specific and important application driving the use of higher spectrum in combination with lower spectrum. Hence, the JCAS specifics, at digital or RF level, may benefit from synergies with the 3 topics above.	SNS JU, piggybacking on existing work on JCAS	1, piggybacking on ongoing work
Topic 8. New spectrum and associated challenges (co-existence)	This drives spectrum co-existence and operations of a radio front end optimally to minimize interferences between different users. As such, the required circuitry (to be developed above 10GHz) need to be integrated into an overall system design which should form part of the FEM. Hence the synergy with the previous topics. Strong SNS need to provide the use cases (indoor, outdoor, type of device…)	SNS JU.	2, requires clear definition of the various spectrum bands to aggregate, NTN to be associated

Topic 23. Wide-band amplifiers and integration of several frequency bands	This complements the previous topic by opening operations through the same FEM of a multiplicity of frequency bands, possibly requiring implementations of different techs as a function of the target operation spectrum. Key topic relates to the possibility of reusing lower band circuitry as intermediate stage for higher frequency operations, which implies a comprehensive cross band design. Very important for future multiband devices (including spectrum bands not allocated for terrestrial networks, e.g. Galileo bands)	Chips JU, integration of multiple techs/bands	>2, as per 8. above
Topic 13. Cost-effective III-V Si for power and low-noise amplifier (InP and others)	This is a core topic bringing the designs and technologies defined above closer to realization through bridging the gap with fabrication and development of semiconductors on the most efficient substrates. It brings together the needs of the microelectronics and coms stakeholders closer to realization in Europe.	Chips JU	2. closer to actual implementation.

The above table represents what may be conceived as an initiative towards advanced FEM's for 6G communication systems, with following characteristics to make it strategically credible:

- It mostly piggybacks on EU know-how.
- It consolidates existing work on digital (CMOS) and RF/Power actions as driven by the former KDT JU.
- It has the potential to leverage efforts on pilot lines when implemented by the Chips Act developments (e.g. Pilot Lines on packaging, or on FDSOI, or on 2nm nodes).
- It has potential for international collaboration (e.g. spectrum management).
- It potentially strengthens EU's position on terminal/FEM technologies.

- Whilst it originates from the infrastructure side, it could alleviate risks and facilitate investments by also covering the terminal/device (beyond smartphone) side, which represents a potentially huge market driving foundry use.
- Whilst it may not be possible to address all digital components of a SoC before 3GPP has identified the technological content of 6G (Release 20 and beyond), it can foster EU positions in that respect.

From an operational perspective, the complementarity of topics between SNS and Chips JU could be organized through a combined/synchronized call (synergy call) or through calls pointing at each other but with a different timing if time synchronization is not achievable. The initiative would consist in the above building blocks, to be further developed, and with each JU clearly calling for participation of stakeholders from the other, such that the links requirements/specifications towards technology assessment and integration can be efficient. See also suggested an implementation roadmap in the **Report Appendix**. The appendix suggests a complementary implementation of topics over 3 years under an initiative equally shared by the Chips and SNS JU's, and building up over time from 2025 to 2027. This suggests synchronization of parallel and consecutive Work Programmes (WPs) over 3 years, starting with WP 2025 for the two JU's. For this first WP, a tentative planning is suggested below.

Table 2: Tentative planning for cooperation for the WP 2025

SNS JU	Chips JU
Common understanding to be reached among JU offices, public and private side by mid Feb24	
April 24: SNS WP 2025 Option paper and 1st consultation	SNS option paper to take into account by Chips JU position/status
End of May 24: First draft of WP 2025	Chipset section of SNS draft WP to be reviewed and elaborated with Chips JU
Mid-June 24: SRG meeting	SRG meeting position to be communicated to Chips JU PAB to seek common public understanding
End of June 24: 2nd draft of WP 2025 End of July 24: 2nd Consultation with 6G-IA members	2nd Draft chipset part to be elaborated jointly with Chips JU/Aeneas and consultation extended to Chips JU stakeholders (chipset part)
End of September: 2nd SRG meeting	PAB position requested to seek common position at MS level during SRG meeting

Mid October, Final version.	Coordinated with Chips JU for chipset parts.
Note: as it may take more time to agree WP 2025 in the Chips JU environment, the final SNS version may include a disclaimer "pending final approval at Chips JU level". However, the SNS WP 2025 proposal as described in the Report Appendix below could be implemented with a reasonable level of independence. It is only its final impact that would depend on complementary Chips JU actions.	

5.3. OTHER POSSIBLE INITIATIVES

Other elementary topics can be considered for joint SNS/Chips JU's cooperation, notably:

- Topic 7. Circuit enabling highly-power efficient and dynamically scalable networks. This topic benefits from a reasonable number of contributions and is of high relevance to the sustainability/low energy issues. It could focus on the determination of the energy saving modes in a computing/communication fabric and derive the needed requirements at components level. This could be driven from an SNS perspective owing to the clear system perspective it requires to address, with target proof of concepts to be implemented under the SNS trial streams.
- Topic 16. Integration of photonics and electronics. This topic also benefits from a reasonable number of contributions and optical is seen as an important technology to realize high performances, low energy consumption and where European know how is strong. Focus may however need to be refined, as several approaches may compete, e.g. 2,5/3D integration for in components or across components interconnects, or more classical derivation implying some form of radio over fibre to connects nodes within the network. As TRL 5/6 is targeted, lead could be taken by the Chips JU with possible system demos subsequently handed over to the SNS JU.

For other topics, the following is suggested:

- Topics supported with only one contribution are at this stage not pursued for joint SNS/Chips JU cooperation, but rather addressed independently, if appropriate, in the relevant JU. For instance, a "system topic" like cell free synchronization (Topic 11) could be part of a specific action under SNS.
- A topic like NTN (Topic 20.), which is contributed primarily from the perspective of on-board RF front end technology, could be considered by ESA and other EU Space Agencies. On board technologies are extremely expensive due to their limited market (even if constellations are deployed) and may impose a too high burden on JU's resources with also the need to consider space qualified technology. For other NTN issues such as unification of Radio access and AI piloted waveforms (e.g. Centric project presented at the workshop) the issue could be part of the FEM initiative proposed above.
- Similarly, it seems that the topic like beamformers (Topic 22.) could be integrated under the FEM initiative in the context of SoC and integration of heterogeneous components (Digital vs RF).

In summary, the proposed approach with one framing joint initiative should allow in the short medium term to:

- focus on transceiver technologies and FEM. Target integration of mixed technologies, including Digital and Analog parts for core 6G transceiver capabilities.
- Focus L1 tech solutions and architectures on solutions that benefit from Pilot lines developments in non-R&I contexts (Chips Act capacity building chapter, IPCEI's).
- Adopt sustainability by design approaches for design and development of 6G components.
- develop specific packaging know how and capabilities for heterogeneous hybrid components, in particulars 6G SoC's for radio access networks and possibly some UE types.

include work on EDA tools in view of fostering the implementation through supported pilot lines.

6. COMPUTING AND PROCESSING ISSUES

In the context of digital design, design for low power, starting from SoC architecture through processors to hardware accelerators requires further developments in SRIA plans. With digital SoC's, it represents a domain where Europe has lost capabilities and the skills need to be rebuilt from scratch, including university collaborations to ensure the proper skilling of future workforce, and reducing the cost/risk for companies to insource SoC development with the goal of ensuring EU technological sovereignty.

In that context, the need of open platform is recognized by the few contributions addressing the topic, notably to be able to fulfil security, resilience, trustworthiness and efficiency of a disaggregated platform. RISC-V is one possible solution for an open architecture. Activity in this domain may be more efficient if focusing on the needed application specific addons. Switching and data stream accelerators are mentioned as important aspects under an SNS umbrella. Multi-platform accelerators are seen as an interesting move. It may be needed to fulfil the needs of an energy efficient, trustworthy, and performance-oriented solution of the future. By this the integration of diverse accelerators into disaggregated RAN computing and signal processing hardware will be important. Europe may have an interest to work on an open platform with dedicated accelerators, but this requires to clearly define a market valorisation approach, and it should be noted that the issue is controversial among actors as a function of their current market position.

Regarding an open (e.g. RISC-V) platform, it is mentioned that 3 areas could be considered:

1. As a replacement for L3/L2 compute today using x86 or ARM clusters. There are currently initiatives to lift RISC-V to this class of processors. The software ecosystem is the main drawback. Other business models can be a benefit. Conversely, it could be envisaged that RISC-V developments in the Software Defined Vehicle supported

under the Chips Act could be synergized with such an activity. These applications are though those at CU or DU level and not necessarily the most challenging from a computing perspective.

2. Replacement of ARM M class control cores, straight forward already today. ARM license models are quite costly, and RISC-V may be an alternative.
3. Integrated in an evolved/new proprietary architecture. RISC-V supports features which would be good for L1 and BF compute, but this entails big challenges (e.g. streaming of data in L1 and BF processing). Lots of the processing in L1 and BF (and DFE) is of a streaming nature with high bandwidth and high real-time requirements. Feasibility and cost efficiency are though not granted. In general, it is well accepted that high real time requirements with massive RT computing needs may not be served by standard processors and will require some level of purpose-built processors, e.g. with ASICs.

Regarding accelerators, it is indicated that there will probably be a market for more widespread accelerators for AI (many variants), Analog neural networks inference processing, Crypto, packet processing, compression, etc. It is though unlikely that there will be a generic market for telco accelerators like LDPC. The market is too small and leading vendors make their own custom silicon for this purpose.

6.1. MOVING FORWARD ON COMPUTING

Whilst RISC-V architecture appear to gain grounds in several application domains, its place within the communication sector is just emerging. The report[7] *"Recommendations and Roadmap for European Sovereignty in Open-Source Hardware, Software, and RISC-V Technologies"* handed over by industry to the Commission indicate that: "*RISC-V is expected to be a key driver for new IC's developed for personal devices and communication infrastructure*." In this report, the role and importance of application specific accelerators is also noted, together with the open interfaces they offer to computing resources. A possible approach in this domain could include:

First phase:

- Define an accelerator centric initiative, that will focus on core functions (ML, cryptography…) to be accelerated on virtualized platforms from an efficiency and trustworthiness perspective. Many domains can be defined, and an open-source approach would here benefit from existing EDA tools. Existing platforms may be considered in that respect, but industrial choices may need further elaboration considering that different accelerator strategy are contemplated by industry, like GPU (Nvdia), FPGA (Intel), DSP (Qualcomm), Nokia ML/AI Chip development. The current SNS BeGreen project is considering ARM as a target platform, but a more strategic top-down approach may be considered, including also other European players.

[7] https://digital-strategy.ec.europa.eu/en/library/recommendations-and-roadmap-european-sovereignty-open-source-hardware-software-and-risc-v

- In parallel assess the opportunity of developing RISC-V modules in complement of the work currently on going under the Chips JU and in the context of the Software Defined Vehicle. As the Chips JU concentrates on generic modules, the complementary work could target specific communication modules taking as application, in a first step, CU and DU capabilities (less demanding than RT capabilities). Although these are already covered by existing platforms (e.g. Intel FlexRan), it may add value from 2 different perspectives: i) by bringing additional open capabilities with focus on innovation; ii) by focusing design and architecture on trustworthiness, in the wake of the CoreNext project, in addition to performance that is the primary design parameter considered by existing platforms.

Second Phase

- Further study the opportunity to extend the RISC-V module capabilities beyond CU/DU capabilities and address critical RU Real Time function through dedicated accelerators, developed for the RISC-V platform. This would imply an extension of both items of the first phase, in view of further developing trustworthy high-performance digital multiprocessors, with a focus on open technology.
- Alternatively, stimulate joint work (international cooperation work) with other industries to address L2 and above processing in an optimized manner, including issues like packet switching and forwarding.

From a JU cooperation perspective, the development of phase 1 interoperable accelerators could be addressed by the SNS JU whilst the development of RISC-V modules for communication could be part of the Chips JU, piggybacking on the RISC-V developments of the Software Defined Vehicle.

For the second phase, the partitioning of efforts remains for further study as it would highly depend on results of phase 1.

These digital developments may benefit from a common coordination mechanism between the SNS/Chips JU in view of stimulating the various developments from an industrial perspective, including planning for future IPCEI's as appropriate.

7. REPORT APPENDIX – FEM INITIATIVE SUGGESTED IMPLEMENTATION PLANNING

	WP 2025	WP 2026	WP 2027
SNS WP	A) **Topic 3. High throughput/capacity fronthaul** 100 Gbps digital data path moves the integration work one step closer of SoC's, as devices where the added value is. Moves into the domain of digital function designs, though constrained at layer 1. **B) Topic 6. Joint Communication and Sensing** application driving the use of higher spectrum in combination with lower spectrum. JCAS specifics, at digital or RF level.	Topic 8.**New spectrum and associated challenges** (co-existence). This drives spectrum co-existence and operations of a radio front end optimally to minimize interferences between different users. As such, the required circuitry (to be developed above 10GHz) need to be integrated into an overall system design which should form part of the FEM.	TBD, tentatively a CSA to prepare transfer to Pilot Lines, in combination with Chips JU.
Notes SNS	**A)** Focus on system perspective with definition of functions in SoC. To be later continued and expanded in subsequent	SNS need to provide the use cases (indoor, outdoor, type of device…) and to involve NTN community for FR3 co-existence.	

	phases. Prepares for high level of node integration for further transfer to Pilot Lines. **B)** Implementation aspects of a combined Rx/Tx chain for JCAS with high node integration.		
Synchro	**A)** In call identification of Chips JU Digital developments, notably for mmWave fronthaul, which may be expanded to answer the call. May include participation clause with parts restricted to Chips JU IA members (as done for 6G-IA members). **B)** Call to include clause for leveraging Chips JU developments	Sequential: delivers downstream requirements to CJU community	
Chips JU WP	**Topic 1. Ultra-high transmit power/system** Core technologies to develop high power/ high gain/low noise transceivers together with their coupling with CMOS digital technology. This is a core building	**A) Topic 2. mmWave Radio integration system in a package,** heterogeneous integration Focus is on heterogeneity of technologies, their integration and packaging. Not a strong EU point, important from the	**Topic 23. Wide-band amplifiers and integration of several frequency bands** opening operations through the same FEM of a multiplicity of frequency bands, possibly requiring implementations of different techs as a function of the target operation

	block for power/energy efficient operation at beyond mmWwave frequency bands.	competitiveness perspective, with focus on com Front End of 5G/6G. **B) Topic 13. Cost-effective III-V Si for power and low-noise amplifier** (InP and others) This is a core topic bringing the designs and technologies closer to realization through bridging the gap with fabrication and development of semiconductors on the most efficient substrates.	spectrum. Key topic relates to the possibility of reusing lower band circuitry as intermediate stage for higher frequency operations, which implies a comprehensive cross band design. Very important for future multiband devices (including non coms, e.g. Galileo bands…)
Notes Chips JU	Focus on elementary technologies as building blocks of Transmitter Receiver Modules with high gain, low noise, low energy and coupling with Digital control capabilities. This may leverage Chips JU (former KDT) work at mm Wave	**A)** Goes beyond or leverages Focus topic of Chips JU on THz coms packaging and prepares for future transfer to Pilot Line. **B)** Follow up of topic 1 that prepares transfer to Pilot Lines.	Expansion of topic 8 addressed by SNS, closer to implementation.
Synchro	Chips JU call to point at core 6G tech for RAN and indicate in call the relation to SNS developments (or other 6G initiatives), ideally building up on those.	A)To be defined in 2025	Piggybacking on SNS topic 8 TBD

8. ANNEX 1: COMPLETE LIST OF TOPICS FOR COMBINED MICROELECTRONICS-TELECOM R&I WORK IN THE 6G CONTEXT AS PRODUCED DURING THE F2F WORKSHOP

1. Ultra-high transmit power/system gain beyond 100 GHz
2. mmWave Radio integration system in a package, heterogeneous integration
3. High throughput capacity/fronthaul 100 Gbps digital datapath
4. Sustainability by design
5. Low-power solution for IoT/backscattering, zero-power for radars
6. Joint Communication and Sensing
7. Circuit enabling highly-power efficient and dynamically scalable networks
8. New spectrum and associated challenges (co-existence)
9. Fabrication technologies for efficient mmWave wireless systems
10. Technologies for self-interference cancellation (full-duplex and monostatic sensing)
11. Cell-free architecture sync and estimation of position and orientation (for infrastructure)
12. SiGe process platform for mmWave and sub-THz radio (including EDA)
13. Cost-effective III-V Si for power and low-noise amplifier (InP and others)
14. FDSoI platform for digital processing (including EDA)
15. Power-efficient architectures e-2-e
16. Integration of photonics and electronics
17. Versatile networks for mmWave and THz and essential fabric (fiber optics)
18. Applications (e.g. Beamforming)
19. Physical-layer security for latency and energy constraint systems
20. NTN -
21. Low cost energy efficient solutions for jamming and interference mitigation at the edge
22. Energy efficient mmWave beamforming and signal transfer using new materials, (metamaterial)
23. Wide-band amplifiers and integration of several frequency bands
24. Integrated radio including interfaces component disaggregation
25. Analog neural networks inference processing for 6G air interface, edge and 3rd gen UEs (Metaverse)

9. ANNEX 2: LIST OF PARTICIPANTS TO THE WORKSHOP ON 16 OCTOBER 2023

Surname	*Name*	*Company / Institute / University*
Achouche	Mohand	NOKIA
Barani	Bernard	6G-IA
Belot	Didier	ST - Microelectronics
Bourdoux	Andre	IMEC
Bourse	Didier	NOKIA
Bueno	Javier Albares	SNS JU
Carli	Anna-Caterina	DG-CNECT (excused)
Cogez	Patrick	AENEAS
Desling	Jerger	LTU – ECS Connectivity chapter editor
Diaz-Pines	Agustin	DG-CNECT
Fournogerakis	Pavlos	SNS JU
Fribourg-Blanc	Eric	Chips JU
Ghoraishi	Mir	Gigasys
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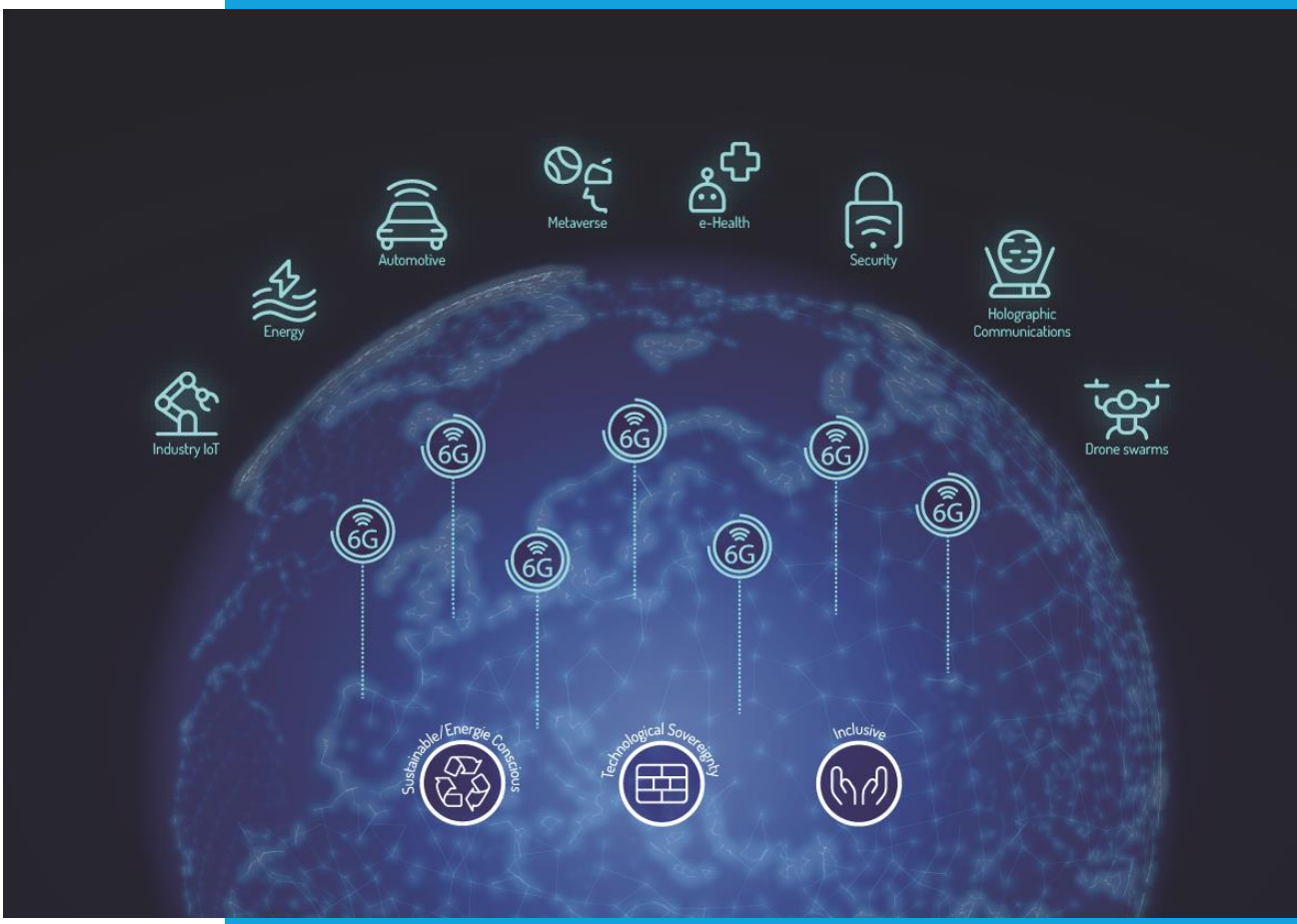

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